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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/535,476
Filing Date: May 17, 2005
Appellant(s): BRAGAGNINI ET AL.

Jordan N. Bodner
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed February 10, 2011 appealing from the Office action mailed August 30, 2010.

(1) Real Party in Interest

The examiner has no comment on the statement, or lack of statement, identifying by name the real party in interest in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The following is a list of claims that are rejected and pending in the application:

Claims 1, 3-9, and 11-15 are pending.

Claims 2 and 10 are cancelled.

Accordingly, the claims on Appeal are 1, 3-9, and 11-15.

(4) Status of Amendments After Final

The examiner has no comment on the appellant's statement of the status of amendments after final rejection contained in the brief.

(5) Summary of Claimed Subject Matter

The examiner has no comment on the summary of claimed subject matter contained in the brief.

(6) Grounds of Rejection to be Reviewed on Appeal

The examiner has no comment on the appellant's statement of the grounds of rejection to be reviewed on appeal. Every ground of rejection set forth in the Office action from which the appeal is taken (as modified by any advisory actions) is being maintained by the examiner except for the grounds of rejection (if any) listed under the subheading "WITHDRAWN REJECTIONS." New grounds of rejection (if any) are provided under the subheading "NEW GROUNDS OF REJECTION."

(7) Claims Appendix

The examiner has no comment on the copy of the appealed claims contained in the Appendix to the appellant's brief.

(**8) Evidence Relied Upon**

5,781,799	Leger, et al.	07-1998
2003/0033454	Walker et al.	02-2003
6,870,929	Greene	05-2005

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1, 3-9 and 11-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Leger et al. (US 5,781,799), hereafter referred to as Leger'799 in view of Walker et al. (US

2003/0033454), hereafter referred to as Walker'454 and Greene (US 6,870,929), hereafter referred to as Greene'929.

Referring to claim 1, Leger'799 teaches a method of exchanging data within a direct memory access arrangement including a plurality of IP blocks (plurality of communication sources such as disk controllers, SCSI controllers, parallel data ports, LANs and WANs, column 4, lines 7-9), the method comprising the steps of: associating with said IP blocks respective DMA modules (DMA controllers 20 each with multiple channels as seen in figure 1 and column 4, lines 2-3); and coupling said respective DMA modules over a data transfer facility in a chain arrangement (DMA controllers 20 in a daisy chain as seen in figure 2 and column 4, lines 38-39).

Leger'799 does not appear to explicitly teach said DMA modules each including an input buffer and an output buffer; the chain wherein each DMA module, other than the last in the chain, has its respective output buffers coupled to the input buffer of another of said DMA modules downstream in the chain and each of said DMA modules, other than the first in the chain, has its respective input buffer coupled to the output buffer of another of said DMA modules upstream in the chain; causing each of said DMA modules to interact with the respective IP block by writing

data from the input buffer of the DMA module into the respective IP block and reading data from the respective IP block into the output buffer of the DMA module; and operating said input and output buffers in such a way that: said writing of data from the input buffer of the DMA module into the respective IP block is started when the respective input buffer is at least partly filled with data, and when said reading of data from the respective IP block into the output buffer of the DMA module is completed, the data in the output buffer of the DMA module are transferred to the input buffer of the DMA module downstream in the chain or, in the case of the last DMA module in the chain, are provided as output data; controlling transfer of data between said coupled buffers over said data transfer facility by: issuing at least one request of a requesting buffer for a buffer coupled therewith to indicate at least one transfer condition selected out of the group consisting of: data existing to be transferred and enough space existing for receiving said data when transferred; issuing at least one corresponding acknowledgement towards said requesting buffer confirming that the said at least one transfer condition is met; and transferring data between said requesting buffer and said coupled buffer, whereby said data transfer facility is left free

between said at least one request and said at least one acknowledgement.

However, Walker'454 teaches each DMA module including an input buffer (data is buffered internally between read and write operations, paragraph 4, lines 6-7) and an output buffer (data is buffered internally between read and write operations, paragraph 4, lines 6-7); causing each of said DMA modules to interact with the respective IP block by writing data from the input buffer of the DMA module into the respective IP block (writing data to destination, paragraph 4, line 3) and reading data from the respective IP block into the output buffer of the DMA module (reading data from source, paragraph 4, line 2); and operating said input and output buffers in such a way that: said writing of data from the input buffer of the DMA module into the respective IP block is started when the respective input buffer is at least partly filled with data (it is inherent to the invention that the buffer be at least partly filled with data while writing into the IP block); and when said reading of data from the respective IP block into the output buffer of the DMA module is completed, the data in the output buffer of the DMA module are transferred to the input buffer of the DMA module downstream in the chain (couple port A to port B, paragraph 30, line 8) or, in the case of the last DMA module in the chain, are

provided as output data (ports coupled to other locations, paragraph 24, lines 1-2); and controlling transfer of data between said coupled buffers over said data transfer facility by: issuing at least one request of a requesting buffer for a buffer coupled therewith to indicate at least one transfer condition selected out of the group consisting of: data existing to be transferred and enough space existing for receiving said data when transferred (DMA modules cannot function properly unless there is a method to confirm that data exists to be transferred and/or enough space exists for receiving the transferred data); issuing at least one corresponding acknowledgement towards said requesting buffer confirming that the said at least one transfer condition is met (bit 8 in transfer size configuration register set to 1, paragraph 37, line 1); and transferring data between said requesting buffer and said coupled buffer (transfer process initiated, paragraph 37, line 2), whereby said data transfer facility is left free between said at least one request and said at least one acknowledgement (read requests can still be made despite busy memory/module, paragraph 38, lines 23-25).

Leger'799 and Walker'454 are analogous art because they are both drawn to the field of direct memory access.

At the time of the invention, it would have been obvious to one of ordinary skill in the art, having the teachings of Leger'799 and Walker'454 before him or her, to modify the method of Leger'799 to incorporate the features of Walker'454 because the addition of an input buffer and an output buffer can facilitate coupling between two DMA modules.

The motivation for doing so would have been to mitigate the typical disadvantage of conventional DMA controllers, wherein said conventional DMA controller acquires complete control of a bus (paragraph 5, lines 1-4; paragraph 6, lines 1-3).

Further, Greene'929 teaches the chain wherein each module, other than the last in the chain, has its respective output buffers coupled to the input buffer of another of said DMA modules downstream in the chain and each of said DMA modules, other than the first in the chain, has its respective input buffer coupled to the output buffer of another of said modules upstream in the chain (combinational sections 804-1 to 804-n and pipeline registers 806-1 to 806-n are parts of each clocked cipher stage 802-1 to 802-n as seen in figure 8 and column 2, lines 10-13; figure 8 shows the pipeline registers 806-1 to 806-2 connected to the combinational sections 804-2 to 804-n respectively); and associating with said input buffers coupled in the chain at least one intermediate block to control data

transfer between said coupled buffers (scheduler 106 controls the order in which data is processed as seen in figure 1 and column 5, lines 32-33).

Greene'929 is analogous to Leger'799 and Walker'454 because they are both drawn to the inventive field of data processing.

At the time of the invention, it would have been obvious to one of ordinary skill in the art, having the teachings of Greene'929, Leger'799 and Walker'454 before him or her, to modify the data-exchanging method of Leger'799 and Walker'454 to include the combinational sections and pipeline registers of Greene'929 because the chain of combinational sections and pipeline registers can enhance the overall performance of the data processing and transfer.

The motivation for combining these teachings would have been to provide a higher throughput (column 2, lines 42-43).

Therefore, it would have been obvious to combine Greene'929 with Leger'799 and Walker'454 to bring about the invention as claimed above.

Note that claim 9 contains the corresponding limitations of claim 1 as shown above; therefore, it is rejected using the same reasoning accordingly.

As to claim 3, Walker'454 teaches the method of claim 1, further comprising the steps of: including a CPU in the arrangement (processor 7, paragraph 33, line 1); using said CPU for transferring data to be processed into the input buffer of the first DMA module in said chain (processor 7 issues a data instruction to DMA controller 5 and writes the source address to the source configuration register, paragraph 33, lines 1-5); and using said CPU for collecting said output data from the output buffer of the last DMA module in said chain (processor 7 issues a data instruction to DMA controller 5 and writes the destination address to the destination configuration register, paragraph 33, lines 1-5).

Note that claims 5, 11 and 14-15 contain the corresponding limitations of claim 3 as shown above; therefore, they are rejected using the same reasoning accordingly.

As to claim 4, Walker'454 teaches the method of claim 3, further comprising the step of: configuring said DMA modules via said CPU (processor 7 issues data transfer instructions containing source address and destination address to DMA controller 5, paragraph 33, lines 1-4).

As to claim 6, Walker'454 teaches the apparatus of claim 5 wherein at least one of said input and output buffers has a fixed data width with respect to said data transfer facility (consistent data width regarding bus transfers is inherent to proper functionality of DMA modules) and a selectively variable data width with respect to said respective IP blocks (variable buffer size parameters bits 4:2 in source and destination configuration registers, paragraph 33, line 10 - paragraph 34).

Note that claim 13 contains the corresponding limitations of claim 6 as shown above; therefore, it is rejected using the same reasoning accordingly.

As to claim 7, Walker'454 teaches the apparatus of claim 5, further comprising: a slave interface module (processor 7, paragraph 33, line 1) configured to read from outside the apparatus data relating to at least one parameter selected from the group consisting of: a parameter indicating how many bits are available in at least one of said input buffers (size of the data block to be transferred, paragraph 36, lines 1-2); a parameter indicating how many bits are present in at least one of said input buffers (destination address register buffer size bits 4:2, paragraph 34); a parameter indicating how many bits

are available for reading in at least one of said output buffers (source address bits 31:10, paragraph 33, line 10); and a parameter indicating how many bits are present in at least one of said output buffers (source address register buffer size bits 4:2, paragraph 33, line 10).

As to claim 8, Walker'454 teaches the apparatus of claim 5 further comprising: a reprogrammable finite state machine (state machine 6 as seen in figure 3 and paragraph 31, line 4) configured to drive operation of said apparatus by receiving data from at least one of said input buffers (data is buffered internally between read and write operations, paragraph 4, lines 6-7), downloading data into said respective IP block corresponding to said at least one of said input buffers (write the data to the destination, paragraph 4, line 3), receiving data from said respective IP block (read the data from the source, paragraph 4, line 2), and storing data in said at least one of said output buffers (data is buffered internally between read and write operations, paragraph 4, lines 6-7).

As to claim 12, Leger'799 and Walker'454 do not teach the apparatus of claim 11, wherein the plurality of DMA modules comprises three DMA modules. However, an apparatus comprising

three DMA modules is simply an alternative arrangement in the art.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify Leger'799 and Walker'454's system to incorporate, as shown above, the apparatus of claim 11, wherein the plurality of DMA modules comprises three DMA modules. The motivation to combine these teachings is to enable other modules to access the system bus while a DMA controller is handling a transfer between two modules (paragraph 5, lines 2-6).

(10) Response to Argument

Applicant's Argument (page 11, line 3 - page 12, line 14)

Referring to claim 1, Applicant argues that Leger and Walker would not have obviously been combined to bring about coupling DMA modules, since Walker does not explicitly teach chaining together multiple DMA controllers, or that other modules could be other DMA controllers (page 11, line 3 - page 12, line 14).

Examiner's Response

Examiner respectfully submits that Leger teaches the chaining together of multiple DMA components, while Walker

teaches the DMA controller handling a transfer between two locations, such as a processor, memory, or bus, without occupying the system bus. Examiner likewise respectfully submits that duplication of components is a well-understood practice in the art, and that Walker was teaching a more general method of transferring data between two modules through a single DMA controller. With these in mind, it is not reasonable to presume that the data being transferred is transferred between two separate DMA controllers through a third DMA controller.

Applicant's Arguments (page 12, line 15 - page 13, line 9)

Further, Applicant argues that the stated obviousness is a circular argument, and that the motivation does not explain why or how one would arrive at DMA modules coupled together as claimed (page 12, line 15 - page 13, line 9).

Examiner's Response

Examiner respectfully submits that it would have been obvious to combine the teachings of Leger and Walker because duplication of components is a common and well-understood practice in the art, and that Walker teaches general modules being coupled through the DMA controller.

Applicant's Arguments (page 14, line 1 - page 15, line 8)

Further, Applicant argues that combining Greene with Walker and Leger would not have sped up the throughput of a DMA system, or even be expected to work at all (page 14, line 1 - page 15, line 8).

Examiner's Response

Examiner respectfully submits that, as shown in figure 5 of Greene, the invention of Greene has an input buffer/working store 504, an encryption section 506, and an output buffer 508. One of ordinary skill in the art could reasonably swap out the encryption section for a DMA section to repurpose the component as a DMA controller. Further, improved pipelines are not necessarily slow, and indeed a pipelined DMA system in which each DMA controller handles a respective device or set of device would be faster than one DMA controller having to handle every device.

Applicant's Arguments (page 15, line 9 - page 16, line 9)

Further, Applicant also argues that there is no valid reason cited as to why one would want to add encryption to a DMA system in the first place, that "pipelining often slows processes down", and that Greene is directed to a very different

type of data processing from the invention (page 15, line 9 - page 16, line 9).

Examiner's Response

Examiner respectfully submits that Greene was not mentioned to add encryption to a DMA system, but rather to point out a system in which components were daisy-chained together in such a way as that an output buffer of a first component was connected to an input buffer of a second component. As stated above, one of ordinary skill in the art could reasonably swap out the encryption system in favor of a DMA section so as to repurpose the component as a DMA controller. Further, Applicant has not cited any specific incidents in which pipelining slows processes down.

Further, referring to independent claims 5 and 11, Applicant's arguments are fundamentally indistinct from those referring to independent claim 1 as shown above; therefore, they are answered using the same reasoning accordingly.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/JOHN B. ROCHE/

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